

IRFB4110PbF

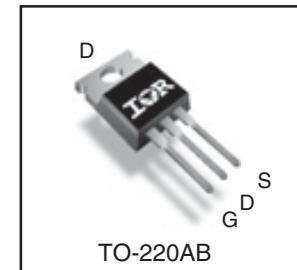
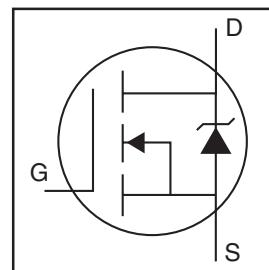
Applications

- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits

- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and di/dt Capability

HEXFET® Power MOSFET	
V_{DSS}	100V
R_{DS(on)} typ.	3.7mΩ
	4.5mΩ
I_D (Silicon Limited)	180A ①
I_D (Package Limited)	120A



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	180①	A
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	130①	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Wire Bond Limited)	120	
I _{DM}	Pulsed Drain Current ②	670	
P _D @ T _C = 25°C	Maximum Power Dissipation	370	W
	Linear Derating Factor	2.5	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ④	5.3	V/ns
T _J	Operating Junction and	-55 to + 175	°C
T _{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Avalanche Characteristics

EAS (Thermally limited)	Single Pulse Avalanche Energy ③	190	mJ
I _{AR}	Avalanche Current ②	See Fig. 14, 15, 22a, 22b	A
EAR	Repetitive Avalanche Energy ⑤		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R _{θJC}	Junction-to-Case ⑥	—	0.402	°C/W
R _{θCS}	Case-to-Sink, Flat Greased Surface	0.50	—	
R _{θJA}	Junction-to-Ambient ⑦	—	62	

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(\text{BR})\text{DSS}}$	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu\text{A}$
$\Delta V_{(\text{BR})\text{DSS}}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.108	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 5\text{mA}$ ②
$R_{\text{DS}(\text{on})}$	Static Drain-to-Source On-Resistance	—	3.7	4.5	$\text{m}\Omega$	$V_{GS} = 10V, I_D = 75\text{A}$ ⑤
$V_{GS(\text{th})}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 100V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 100V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	160	—	—	S	$V_{DS} = 50V, I_D = 75\text{A}$
Q_g	Total Gate Charge	—	150	210	nC	$I_D = 75\text{A}$
Q_{gs}	Gate-to-Source Charge	—	35	—		$V_{DS} = 50V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	43	—		$V_{GS} = 10V$ ⑤
R_G	Gate Resistance	—	1.3	—	Ω	
$t_{d(\text{on})}$	Turn-On Delay Time	—	25	—	ns	$V_{DD} = 65V$
t_r	Rise Time	—	67	—		$I_D = 75\text{A}$
$t_{d(\text{off})}$	Turn-Off Delay Time	—	78	—		$R_G = 2.6\Omega$
t_f	Fall Time	—	88	—		$V_{GS} = 10V$ ⑤
C_{iss}	Input Capacitance	—	9620	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	670	—		$V_{DS} = 50V$
C_{rss}	Reverse Transfer Capacitance	—	250	—		$f = 1.0\text{MHz}$
$C_{oss \text{ eff. (ER)}}$	Effective Output Capacitance (Energy Related)⑦	—	820	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V$ ⑧
$C_{oss \text{ eff. (TR)}}$	Effective Output Capacitance (Time Related)⑥	—	950	—		$V_{GS} = 0V, V_{DS} = 0V \text{ to } 80V$ ⑨

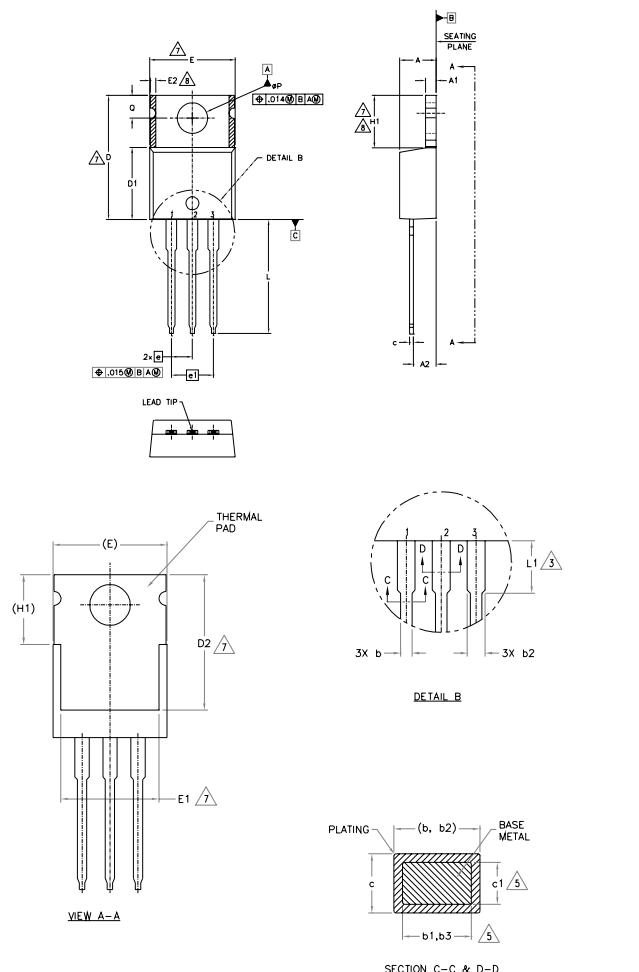
Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	170①	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ②⑦	—	—	670		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 75\text{A}, V_{GS} = 0V$ ⑤
t_{rr}	Reverse Recovery Time	—	50	75	ns	$T_J = 25^\circ\text{C}$ $V_R = 85V,$
		—	60	90		$T_J = 125^\circ\text{C}$ $I_F = 75\text{A}$
Q_{rr}	Reverse Recovery Charge	—	94	140	nC	$T_J = 25^\circ\text{C}$ $\text{di/dt} = 100\text{A}/\mu\text{s}$ ⑤
		—	140	210		$T_J = 125^\circ\text{C}$
I_{RRM}	Reverse Recovery Current	—	3.5	—	A	$T_J = 25^\circ\text{C}$
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 120A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by $T_{J\text{max}}$, starting $T_J = 25^\circ\text{C}$, $L = 0.033\text{mH}$
 $R_G = 25\Omega, I_{AS} = 108\text{A}, V_{GS} = 10V$. Part not recommended for use above this value.
- ④ $I_{SD} \leq 75\text{A}$, $\text{di/dt} \leq 630\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(\text{BR})\text{DSS}}$, $T_J \leq 175^\circ\text{C}$.
- ⑤ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑥ $C_{oss \text{ eff. (TR)}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑦ $C_{oss \text{ eff. (ER)}}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ R_θ is measured at T_J approximately 90°C .

TO-220AB Package Outline (Dimensions are shown in millimeters (inches))



NOTES:

- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1
- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
- CONTROLLING DIMENSION : INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
- DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRRREGULARITIES ARE ALLOWED.
- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES	
	MILLIMETERS		INCHES			
	MIN.	MAX.	MIN.	MAX.		
A	3.56	4.83	.140	.190		
A1	0.51	1.40	.020	.055		
A2	2.03	2.92	.080	.115		
b	0.38	1.01	.015	.040		
b1	0.38	0.97	.015	.038	5	
b2	1.14	1.78	.045	.070		
b3	1.14	1.73	.045	.068	5	
c	0.36	0.61	.014	.024		
c1	0.36	0.56	.014	.022	5	
D	14.22	16.51	.560	.650		
D1	8.58	9.02	.330	.355		
D2	11.68	12.88	.460	.507	7	
E	9.65	10.67	.380	.420	4,7	
E1	6.86	8.89	.270	.350	7	
E2	—	0.76	—	.030	8	
e	2.54 BSC		.100 BSC			
e1	5.08 BSC		.200 BSC			
H1	5.84	6.86	.230	.270	7,8	
L	12.70	14.73	.500	.580		
L1	3.56	4.06	.140	.160	3	
OP	3.54	4.08	.139	.161		
Q	2.54	3.42	.100	.135		

LEAD ASSIGNMENTS

- HEXFET
1. GATE
2. DRAIN
3. SOURCE

IGBTs, C-PACK

1. GATE
2. COLLECTOR
3. Emitter

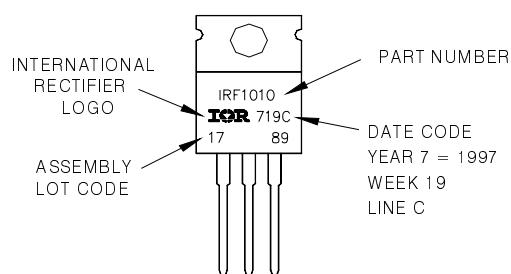
DIODES

1. ANODE
2. CATHODE
3. ANODE

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE 'C'

Note: "P" in assembly line position indicates "Lead-Free"



TO-220AB packages are not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.

International
IR Rectifier